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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,471	03/30/2004	Jung Ta Chang	CHAN3246/EM	3261

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EXAMINER	
UNELUS, ERNEST	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,471	CHANG ET AL.	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
11/21/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

I. CLAIMS REJECTIONS BASED ON PRIOR ART

Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

This new ground of rejection is address below.

II. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

III. INFORMATION CONCERNING DRAWINGS

Drawings

5. The applicant's drawings submitted are not acceptable for examination purposes.

IV. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US pub. 2004/0182938) in view of Kimura (US pat. 5,625,593).

8. As per **claim 1**, Chen discloses a memory card having a plurality of different interfaces **(an MS, SD, and a USB, see paragraph 0034)**, comprising: a function module **(the voltage transformation/protection circuit 85 in fig. 8)**; a controller **(micro controller 83 in fig. 8)** coupled to the function module for accessing **(see fig. 8)**; including a detection/switching circuit, a first and second signal with a first and second voltage when the card is inserted **(see paragraph 0021)**, and wherein the memory card separate two of the interfaces by activating one of the interfaces for detecting the first voltage level when the memory card is inserted into a first card reader **(see paragraph 0021)**, but fails to disclose expressly "a first buffer coupled to the controller for sending a first control signal, the first buffer including a pull-down resistor for providing a first voltage level; and a second buffer coupled to the controller for sending a second control signal, the second buffer including a pull-up resistor for providing a second voltage level, wherein the memory card uses the pull-down and the pull-up resistors to separate two of the interfaces by activating one of the interfaces for detecting the first voltage level of the first buffer when the memory card is inserted into a first card reader, such that the first buffer is activated to send the first control signal if the detection of the first voltage level of the first buffer is positive; or by activating another interface for detecting the second voltage level of the second buffer when the memory card is inserted into a second card reader, and such that the second

buffer is activated to send the second control signal if the detection of the second voltage level of the second buffer is positive".

Kimura discloses "a first buffer **(buffer 18a)** for sending a first control signal **(see fig. 2)**, the first buffer including a pull-down resistor **(pull-down resistor 22)** for providing a first voltage level **(see fig. 2 and col. 6, line 15 to col. 7, line 15)**; and a second buffer **(buffer 18b)** for sending a second control signal **(see fig. 2)**, the second buffer including a pull-up **(pull-up resistor 22)** resistor for providing a second voltage level **(see fig. 2 and col. 6, line 15 to col. 7, line 15)**, such that the first buffer is activated to send the first control signal if the detection of the first voltage level of the first buffer is positive **(see fig. 2 and col. 6, line 15 to col. 7, line 15)**; or by activating another interface for detecting the second voltage level of the second buffer when the memory card is inserted into a second card reader, and such that the second buffer is activated to send the second control signal if the detection of the second voltage level of the second buffer is positive".

Chen et al. (US pub. 2004/0182938) and Kimura (US pat. 5,625,593) are analogous art because they are from the same field of endeavor of memory card.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify a memory card adapter supporting different memory cards, said adapter consolidates specifications, dimensions, and circuits of different memory cards into a single all-in-one read/write slot and is connected to a computer system via a transmission interface (e.g., USB, IEEE1394, PCMCIA, CF) to enable data transmission as taught by Chen and a memory card circuit according to the present invention is provided in a portable card medium and when

the card medium is inserted into a terminal unit, it is electrically connected with the terminal unit to process data as taught by Kimura.

The motivation for doing so would have been because Chen teaches that **"The interface detection/switching circuit 82 comprises detection circuit 821, switching circuit 822, and MF1 and MF2 pins of common transmission interface 81, wherein the detection circuit 821 is used to automatically detect the potential variation in initializations signals to determine the type of memory card system interface where said micro memory card 8 is inserted " (paragraph 0030).**

Therefore, it would have been obvious to combine Kimura (US pat. 5,625,593) with Chen et al. (US pub. 2004/0182938) for the benefit of creating the memory card to obtain the invention as specified in claim 1.

9. As per **claim 2**, the combination of Chen and Kimura disclose "the memory card as claimed in claim 1," **(see rejection to claim 1 above)**; Chen further discloses, " wherein the master controller is wherein the one of the interfaces is for a SD card" **(see paragraph 0015).**

10. As per **claim 3**, the combination of Chen and Kimura disclose "the memory card as claimed in claim 1," **(see rejection to claim 1 above)**; Chen further discloses wherein the first voltage level is a high voltage level" **(see paragraph 0024 and fig. 2).**

11. As per **claim 4**, the combination of Chen and Kimura disclose "the memory card as claimed in claim 1," **(see rejection to claim 1 above)**; Chen further discloses wherein the first control signal is a CMD signal" **(see fig. 7)**.

12. As per **claim 5**, the combination of Chen and Kimura disclose "the memory card as claimed in claim 1," **(see rejection to claim 1 above)**; Chen further discloses, "wherein the another interface is for a MS card **(see paragraph 0015)**.

13. As per **claim 6**, the combination of Chen and Kimura disclose "the memory card as claimed in claim 1," **(see rejection to claim 1 above)**; Chen further discloses wherein the second voltage level is a lower voltage level **(see paragraph 0024 and fig. 2)**.

14. As per **claim 7**, the combination of Chen and Kimura disclose "the memory card as claimed in claim 1," **(see rejection to claim 1 above)**; Chen further discloses wherein the second control signal is a BS signal **(see fig. 6)**.

V. RELEVANT ART CITED BY THE EXAMINER

15. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

16. The following reference teaches of a memory card having multiple interfaces.

U.S. PATENT NUMBER

US 2004/0117553

US 7,104,848

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

17. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

18. The instant application having Application No. 10/812,471 had a total of 7 claims pending in the application, all of which have received a final action on the merits.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

20. If attempts to reach the above noted Examiner by telephone is unsuccessful, the Examiner's supervisor, Mr. Fritz M. Fleming, can be reached at the following telephone number: Area Code (571) 272-4145.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 21, 2006

Ernest Unelus
Examiner
Art Unit 2181

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11/21/2006